Hall Ticket Number:

Code No. : 14325

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (E.E.E. : CBCS) IV-Semester Main Examinations, January-2021

Digital Electronics

Time: **2** hours Max. Marks: **60**

*Note: Answer any **NINE** questions from **Part-A** and any **THREE** from **Part-B***

Part-A (9 × 2 = 18 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Reduce the following Boolean expressions to the minimum of literals. (i) A' B' C' + A' B C' + A B' C' + A B C' (ii) A B + A B C + A' B + A B' C	2	2	1	1
2.	Subtract 23 from 46 using 8-bit 1's compliment method.	2	2	1	1
3.	What is Priority Encoder?	2	1	2	1
4.	Write the Truth Table for Half Subtractor.	2	2	2	1
5.	Compare Latches and Flipflops.	2	1	2	1
6.	Write down the Characteristic Table, Characteristic Equation and Excitation Table for T- Flip Flop.	2	2	2	1
7.	What are different types of Analog to Digital (A/D) Converters?	2	2	3	1
8.	What are the Applications of Digital to Analog (D/A) Converters?	2	2	3	1
9.	What are different types of PLDs?	2	1	4	1
10.	What is FPGA?	2	2	4	1
11.	Convert the hexadecimal number 4B5 to (i) Octal number (ii) Decimal number	2	1	1	1
12.	Draw the full adder logic circuit with two half adders.	2	1	2	2
	Part-B (3 × 14 = 42 Marks)				
13. a)	The hamming code messages (i) 1101101 (ii) 0011011 are received. Three parity bits were used in the message for even parity. Detect and correct if any errors are found in the messages.	10	4	1	2
b)	Briefly explain Error Detecting Codes.	4	2	1	1
14. a)	Design a code converter that accepts 3-bit Binary Code as input and generates 3-bit Gray Code as output.	7	3	2	2
b)	Implement $(A, B, C, D) = (1, 3, 4, 11, 12, 13, 14, 15)$ using 16*1 Mux and 8*1 Mux.	7	4	2	2

Contd... 2

Code No. : 14325

15. a)	Design a 3- bit Synchronous counter using JK Flip Flops	7	4	2	2
b)	Explain briefly about the Serial In and Parallel Out Shift Register, with a neat diagram	7	2	2	1
16. a)	With the help of circuit diagram, explain the working principle of a Dual Slope Analog to Digital (A/D) converter.	10	2	3	1
b)	What are the applications of Analog to Digital (A/D) converters?	4	2	3	1
17. a)	Design an Excess-3 to BCD code converter using a PLA.	10	4	4	2
b)	Compare PLA and PAL.	4	3	4	1
18. a)	Draw Logic diagrams and Explain the implementation of below logic gates with NAND gates.(i)AND (ii)OR (iii)X-oR gates	7	2	1	2
b)	Reduce the following expression using 4 variable K map. $F= \sum m(0,1,2,3,5,7,8,9,10,12,13) + d(14,15)$ and implement using logic gates.	7	4	2	2
19.	Answer any ***two*** of the following:				
a)	With the aid of external logic, convert D type flip-flop to a JK flip-flop.	7	2	2	1
b)	Draw the circuit diagram of R - 2R Ladder Digital to Analog (D/A) converter and explain its working principle.	7	2	3	1
c)	Reliaze the following Boolean functions using PAL. (i) $F1(w,x,y,z)= \Sigma m(0,1,2,3,7,9,11)$ (ii) $F2(w,x,y,z)= \Sigma m(0,1,2,3,10,12,14)$	7	3	4	1

M: Marks; L: Bloom's Taxonomy Level; CO: Course Outcome; PO: Programme Outcome

S. No.	Criteria for questions	Percentage
1	Fundamental knowledge (Level-1 & 2)	57
2	Knowledge on application and analysis (Level-3 & 4)	43
3	*Critical thinking and ability to design (Level-5 & 6) (*wherever applicable)	0

*****